

REMARKS

Claims 1-25 are pending. Claims 1-9, 13-18, and 22 are rejected. Claims 10-12, 19-21, and 23-25 were objected to but allowable if amended to incorporate base claim and intervening claim limitations. The allowability of claims 10-12, 19-21, and 23-25 is gratefully acknowledged.

Independent claims 1, 9, 13, 18, and 22 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ishiyama (2001/0008544).

Figure 3 in Ishiyama shows a quantization step controller 73 coupled to an input buffer monitor 52 and an output buffer monitor 62. Figure 3 also shows a frame memory 26 and a frame memory 37. However, neither frame memory 26 nor frame memory 37 are coupled to the quantization step controller 73. As noted in paragraph 0055, "A transcoder controller 3 includes input buffer monitor 52 for monitoring said input buffer 21 of the decoder 1 and output buffer monitor 62 for monitoring the output buffer of the encoder 2. There is also provided a quantization step controller 71 for modifying the quantization step in the compression processing of the encoder 2 based on the information from said input buffer monitor 52 and the output buffer monitor 62."

By contrast, independent claim 1 recites "transcoder rate control connected" the "frame buffer" and the "vbv buffer." Claims 9, 18, and 22, recite "wherein the rate reduction factor and the quantizer scale are computed using vbv buffer and frame buffer information." Claim 13 recites "wherein the amount of rate reduction necessary is determined using vbv buffer and frame buffer information."

Ishiyama does not teach or suggest a "transcoder rate control connected" to a frame buffer or using "frame buffer information" to calculate rate reduction. Ishiyama only describes a "transcoder controller 3" that monitors "input buffer 21" and "output buffer 62." The transcoder in Ishiyama is not coupled to any frame buffer and the transcoder does not receive any frame buffer information to calculate rate reduction.

The Examiner also took Official Notice that "Although Ishiyama shows the channel interface and channel rate control contained within the transcoder rate control, it would have been obvious to split the units apart into their individual components." It is agreed that it is often trivial to split apart components into separate components. However, in the instance cited in Claim 1, channel rate control and transcoder rate control are coupled to different components.

As recited in claim 1, a "channel rate control" is "connected to said vbv buffer and said channel interface" and a "transcoder rate control" is "connected to said frame buffer, said encoder, said vbv buffer and said channel rate control." Ishiyama does not describe rate control connected to a frame buffer or rate control connected to a channel interface. As shown in Figure 3, the controller in Ishiyama only monitors an input buffer 21 and an output buffer 40 to provide a quantization factor Q 33.

In light of the above remarks relating to independent claims 1, 9, 13, 18, and 22, the remaining dependent claims are believed allowable for at least the reasons noted above.

Applicants believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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